# Lab Experiment 4

Realization of Carry Look-ahead Adder

4.1 Objective: To design and simulate the carry look-ahead (4-bit)adder in verilog and synthesize using EDA tools

4.2 Software tools Requirement Equipment’s:

Computer with Xilinx and Modelsim Software Specifications:

HP Computer P4 Processor – 2.8 GHz, 2GB RAM, 160 GB Hard Disk

Software’s: Synthesis tool: Xilinx ISE

Simulation tool: Modelsim Simulator

4.3 Prelab Questions

*(write pre lab Q & A in an A4 sheet)*

1. Write the expression for Propagate and generate term in a CLA.
2. List the efficient method for implementing 64- adder using CLA technique?

* 1. Problem: Write a verilog code to implement the 4-bit Carry Look-ahead adder using structural model.

Logic Diagram:

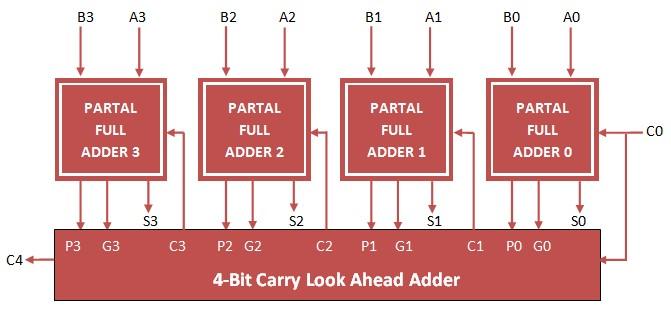


Fig . 4.1 : 4-bit Carry Lookahead Adder

Post Lab:

1. Compare the area, delay and power report of ripple carry & carry look-ahead adder in Xilinx ISE. Create a comparison chart and justify the results.
2. List the application of CLA in VLSI Design.
3. Prepare the synthesis Chart for a 4-bit CLA.
4. Can retiming mechanism improve the speed further in CLA architecture?

**Problem 1:**

**Program: Write a Verilog code to implement the 4-bit Carry Look-ahead adder using s tructural model.**

**Waveform:**

**Carry look-ahead adder:**

**4.6 Result**

Thus, the design of 4-bit carry look-ahead adder circuit was simulated in verilog and synthesized using EDA tool